library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating

---- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity multiplexer is

Port ( i0,i1,i2,i3,i4,i5,i6,i7 : in STD\_LOGIc;

s : in STD\_LOGIC\_VECTOR (2 downto 0);

y : out STD\_LOGIC);

end multiplexer;

architecture Behavioral of multiplexer is

begin

process(i0,i1,i2,i3,i4,i5,i6,i7,s)

begin

case s is

when "000" =>y<=i0;

when "001" =>y<=i1;

when "010" =>y<=i2;

when "011" =>y<=i3;

when "100" =>y<=i4;

when "101" =>y<=i5;

when "110" =>y<=i6;

when "111" =>y<=i7;

when others=>null;

end case;

end process;

end Behavioral;